IN THE SPECIFICATION:

Please amend paragraph number **[0004]** as follows:

[0004] Contact or bond pads 20 on active surface 18 of semiconductor die 16 are electrically and, to an extent mechanically, attached to respective contact pads 24 located on active ~~surface~~ surface 22 of substrate 12 by way of respective bond wires 30 by wire bonding methods known and practiced within the art.

Please amend paragraph number **[0007]** as follows:

[0007] Because there are typically a large number of such solder balls to be contacted by a like number of probes for each chip package which must be arranged in a precise array or pattern in order to make electrical contact with the underlying solder balls, the test tooling is quite expensive, as well as time consuming, to construct. The time and expense factors of providing specific test tooling for each type of BGA chip package having a wide variety of ball grid array patterns is compounded when the particular BGA ~~chips~~ chip packages to be burned-in and tested are of the fine ball grid array variety wherein the balls and spacing are quite small, thereby making the construction of the chip package test tooling even more time consuming and expensive. Furthermore, the specific test tooling to be devised must not only accommodate, burn-in, and test a single chip package, but must also be able to simultaneously accommodate, burn-in, and test a significant number of other chip packages, which may or may not have been segmented from a common substrate and are usually positioned and accompanied by respective cells of test tooling so that production quantities can be produced economically. Thus, it can be appreciated that the time and expense of constructing BGA chip package test tooling which, by necessity, has a multiplicity of probes specifically sized and arranged in patterns which must exactly correspond to the respective solder ball array being tested, are significant hindrances to quickly introducing BGA chip packages and, in particular, FBGA chip packages having new and different solder ball array patterns to the very competitive semiconductor chip marketplace. Furthermore, the test probes of the test tooling must be designed not to unduly damage the solder

balls which will ultimately be used to electrically and mechanically connect the chip package to the next level of assembly by solder ball attachment methods used within the art.

Please amend paragraph number **[0019]** as follows:

[0019] BGA or FBGA semiconductor packages of the present invention generally comprise a substrate having a semiconductor device attached to a selected surface thereof. The semiconductor device has a plurality of bond pads respectively wire bonded to a plurality of bond pads located on the substrate. Preferably, the wire bonds extend through an aperture extending through the substrate. The substrate is further provided with a plurality of circuit traces leading from the substrate bond pads to a plurality of connective elements, such as solder ball contact pads and associated solder balls, which are arranged in a preselected ball grid array pattern. Additional ~~curcuit~~ circuit traces or continuations of the same circuit traces further extend to a plurality of test pads arranged and located on the substrate in a preselected pattern. Preferably, at least the interconnecting circuit traces electrically connecting selected substrate bond pads to intermediately positioned connective elements, preferably including solder ball contact pads and associated solder balls and, in turn, electrically connecting respective test pads are preformed on a tape which can be conveniently and efficiently attached to one or more surfaces of the substrate. Burn-in and testing of the semiconductor chip attached to the ~~substrate is~~ substrate are preferably performed by prior existing test tooling having test probes arranged in patterns typically used in prior known semiconductor chip packages to contact the test pads of the semiconductor chip packages of the present invention. Upon the test pads being contacted by the test probes of the test tooling, selected voltages can be applied to selected pads to burn-in and test the semiconductor device attached to the substrate. This feature is a significant improvement over prior known methods of using test probes specifically designed and arranged in the same specific ball grid array pattern that the individual connective elements or solder balls of prior known ball grid array semiconductor packages are arranged.

Please amend paragraph number **[0021]** as follows:

[0021] Upon successfully burning-in and testing a BGA/FBGA semiconductor package constructed in accordance with the present invention, the test pads may be disassociated from the substrate to decrease the final surface ~~area,~~ area or footprint of the semiconductor package, if so desired.

Please amend paragraph number **[0026]** as follows:

[0026] FIG. 3 is a cross-sectional view of the ball grid array chip package shown in FIG. 1 as taken along section line ~~2/3 - /3~~ 2/3 - 2/3 with encapsulant being disposed over the bond pads located on the active surface of the underlying chip, the bond pads of the substrate, and the interconnecting bond wires;

Please amend paragraph number **[0042]** as follows:

[0042] Referring now to FIGS. 5 and 6 of the drawings, isolated top views of exemplary substrate tape having electrical circuit outlines preformed therein and which are to be applied to one or more exposed faces of a supporting substrate are illustrated. Tapes 50 and 70 shown in drawing FIGS. 5 and 6, respectively, provide a convenient and efficient method of providing circuitry on a supporting substrate in which a chip will ultimately be attached and electrically connected therewith. Each individual chip circuitry portion 51 and 71 is preferably designed to accommodate one chip. Thus, there are multiple, identically repeating individual die portions on a given tape. Such tapes frequently include a thermosetting adhesive which will bond to a wide variety of substrates. The supporting or core substrate may be made from a wide variety of materials with epoxy-glass material such as, but not limited to, bismaleimide-triazine (BT) or ~~FR-4 board~~ FR-4 board, which are both heavily favored by the industry. Alternative substrate materials include ceramic or silicon materials.

Please amend paragraph number **[0044]** as follows:

[0044] Referring to drawing FIG. 5, tape 50 includes an aperture 54 having bond pads 56 located along opposing sides of the ~~aperture.~~ aperture 54. Bond pads 56 are selectively provided with an electrically conductive circuit trace 58 that leads to a respective conductive element, solder ball, or solder ball location 60. Selected conductive elements or solder balls 60 are provided with a second circuit trace 62 leading to a respective test contact pad 64 located outwardly away from aperture 54 and solder balls 60. Test contact pads 64 are preferably arranged to fan out in what is referred to as a thin small outline package (TSOP) which is recognized as an industry standard.

Please amend paragraph number **[0045]** as follows:

[0045] As can be seen in drawing FIG. 5, individual chip circuitry portion 51 includes various circuit traces 58 and 62 which interconnect bond pads 56 to solder balls 60 and which further interconnect solder balls 60 to peripherally located test contact pads 64. Circuit traces 58 and 62 are able to be easily routed around any solder balls 60 in a somewhat serpentine fashion to circumvent one or more particular solder balls that would otherwise physically block the circuit from reaching its respective destination. This particular characteristic of being able to route circuit traces as needed around intervening solder balls 60, or alternative connective elements used in connection with or in lieu of solder balls, allows great versatility in that solder ball grid arrays having virtually any feasible number of solder balls arranged in any feasible pattern could be used and need not be restricted to the exemplary ~~4-column~~ four-column arrangement as shown in drawing FIG. 5. It should be appreciated that although substrate tape 50 provides a convenient, cost-efficient method of providing the desired circuit traces and ball grid array on a selected substrate, alternative methods to apply circuit traces to a substrate can be used. For example, circuit layers including circuit traces, bond pads, solder balls, or contact elements, and/or test contact pads could be screen printed onto one or both faces of a substrate. Furthermore, multiple layers of circuit layers can be disposed upon not only the exposed surfaces

of the supporting substrate but can be "sandwiched" or laminated within the substrate by circuit layer lamination methods known in the art if so desired.

Please amend paragraph number **[0046]** as follows:

[0046] Another exemplary substrate tape 70 showing an individual chip circuitry portion 71 having a preselected ball grid array arrangement is shown in drawing FIG. 6 of the drawings. In drawing FIG. 6, individual chip circuitry portion 71 includes a ~~54-ball~~ 54-ball grid array which has been laid out so as to place solder balls and/or connective elements 80 about the periphery of what is to be ~~thechip-scale~~ the chip-scale package with test contact pads 84 being further outwardly positioned opposite each other along two sides of what will be the chip package. As with test contact pads 64 of the tape outline shown in drawing FIG. 5, test contact pads 84 in drawing FIG. 6 have been prearranged to coincide with a thin small outline package pin-out configuration. Bond pads 76 located along aperture 74 are placed in electrical communication with selected respective solder balls and/or connective elements 80 by circuit traces 78. In turn, selected solder balls 80 are placed in electrical communication with test contact pads 84 through second circuit traces 82 so as to provide a continuous conductive path from a selected test contact pad 84 back to at least one selected bond pad 76.

Please amend paragraph number **[0047]** as follows:

[0047] Collectively referring to drawing FIGS. 7A through 9B, as well as drawing FIGS. 1 through 3, an exemplary BGA chip package constructed in accordance with the present invention is shown in cross-section in drawing FIG. 7A. The process of attaching at least one semiconductor ~~die or device~~ chip or die 92 to the bottom side of a substrate 52, in which an individual chip circuitry portion 51 of tape 50 has been applied to at least the opposite or top side of substrate 52, is carried out much like, if not identical to, prior known methods such as those discussed here with respect to the chip package illustrated in drawing FIGS. 1 through 3. That is, a bare semiconductor chip or die 92 is attached to substrate 52 by way of a die attach adhesive 90. Adhesive 90 is preferably a dielectric adhesive that is nonconductive and has a

coefficient of thermal expansion (CTE) that is compatible with semiconductor die 92. Adhesive 90 may be formed of epoxy resin, polymer adhesives, or any other adhesive having suitable properties. Alternatively, tape having adhesive applied to both sides, such as Kapton™ tape, is particularly suitable for use as die attach adhesive 90. Upon semiconductor die 92 being located and attached to substrate 52 so as to properly orient and align bond pads 56 which are located on the active surface of semiconductor die 92 to face upward within aperture 54 of substrate 52, bond wires 108 are provided which respectively place a selected ~~chip~~ die bond pad 106 in electrical communication with a respectively appropriate bond pad 56 located on the opposite or upper surface of substrate 52. A top view of aperture 54, ~~chip~~ die bond pads 106 located on active surface 104 of semiconductor die 92, bond wires 108, and substrate bond pads 56 can be viewed in drawing FIG. 8A.

Please amend paragraph number **[0048]** as follows:

[0048] Returning to drawing FIG. 7A, it can be seen that an encapsulant 94 has been disposed in and over aperture 54 to cover ~~chip~~ die bond pads 106, bond wires 108, and substrate bond pads 56 in order to provide protection against environmental contaminants, corrosives, and incidental physical contact. Encapsulant 94 may be applied either before burn-in and testing or after burn-in and testing as deemed most appropriate.

Please amend paragraph number **[0049]** as follows:

[0049] Solder balls 60 extend a preselected height above encapsulant 94 to ensure that upon the final chip package being installed on the next level of assembly, encapsulant 94 clears the structure in which solder balls 60 are attached. As practiced within the art, solder balls 60 may be formed of a conductive metal such as gold or may be formed of conductive-filled epoxies having suitable and often very specific conductive properties. Alternatively, solder balls can be attached to the terminal end of a particular circuit trace 58, be attached to contact pads provided on substrate 52 in which a respective circuit trace 58 terminates, or be formed of any type of connective element which can serve in connection with or for the same purpose as a solder ball

which ultimately provides electrical and mechanical attach points on the next higher level of assembly. Furthermore, it will be appreciated by those in the art that substrate 52 may be provided with a multitude of conductive paths and not just the circuit traces shown in drawing FIG. 5. For example, a given solder ball 60 or solder ball location may be in electrical communication with the opposite surface of substrate 52 by way of through-holes or may be in electrical communication with ~~one~~ one or more circuit traces that have been sandwiched or laminated within substrate 52 as known and practiced within the art.

Please amend paragraph number **[0050]** as follows:

[0050] At this stage of construction, the exemplary BGA chip package as shown in drawing FIG. 7A is ready for burn-in and testing and is shown as being detached from tape 50. In accordance with the present invention, semicompleted chip package 66 is then placed in a conventional burn-in and test apparatus which includes test tooling 96 as illustrated in drawing FIG. 7B. ~~A semicompleted~~ A semicompleted BGA chip package 66 is then installed in a chip package holder 98 and a moveable probe head 100 is moved into position as shown by the downwardly pointing arrow of drawing FIG. 7B to carefully engage test contact pads 64 located on the periphery of substrate 52 with complementarily positioned probes 102 that are preferably arranged in the same TSOP pin-out configuration as the underlying test contact pads 64. That is, there is a corresponding probe 102 for each test contact pad 64 that, by way of respective circuit traces 62 and 58, leads to a respective substrate bond pad 56, which, in turn, is in electrical communication with a respective ~~chip~~ die bond pad 106 by way of a bond wire 108, thereby allowing a preselected voltage profile to be applied to initially burn-in attached semiconductor die 92. After burn-in, probes 102 preferably remain in contact with their respective test contact pads 64 and tests are conducted to ensure semiconductor die 92 is fully operational. Optionally, chip package 66 need not be tested immediately after burn-in, but probes 102 and probe head 100 could be withdrawn from chip package 66 and chip package 66 removed from chip package holder 98 to be reinstalled and tested at a later point in time.

Please amend paragraph number **[0054]** as follows:

[0054] Referring now to drawing FIG. 10, illustrated is a side view of an exemplary BGA chip package 110 that is preferably constructed, burned-in, and tested in accordance with the teachings disclosed herein. However, BGA chip package 110 can alternatively be constructed, burned-in, and tested with prior known techniques such as those discussed in relation to drawing FIGS. 1 through 3 herein. As with the exemplary BGA chip packages illustrated in drawing FIGS. 5 through 9B, BGA chip package 110 includes at least one semiconductor die 92 attached to a substrate 112 provided with appropriate electrical traces similar to those provided by way of individual chip circuitry portion 71 of tape 70. However, with respect to chip package 110, a provision must be made to allow for electrical contact to be made through the cross-section of substrate 112 to allow semiconductor die 92 to be attached to the same surface or face of substrate 112 as are solder balls 116 and solder ball contact pads 114. In other words, circuit traces 78 and substrate bond pads 76 are located on what is shown as being the bottom side of substrate 112 in drawing FIG. 10 with circuit traces 78 being placed in electrical communication with the solder ball contact pads 114 located on the opposite side of substrate 112. As mentioned earlier, providing circuit traces on the exposed faces of substrates or, ~~alternatively~~ alternatively, sandwiching the traces within laminated ~~substrates~~ substrates, is known within the art and such can be used to provide electrical communication between solder ball ~~contacts~~ contact pads 114 located on the top surface of substrate 112 with bond pads 76 located on the opposite or bottom side of substrate 112.

Please amend paragraph number **[0058]** as follows:

[0058] Illustrated in drawing FIG. 12 is a cross-sectional view of an exemplary "upside-down" stackable chip package 110 or 110′ as shown in drawing FIGS. 10 and 11. Semiconductor ~~die or device~~ chip or die 92 is positioned on the same side as solder balls 116 with substrate bond pads 76 preferably located on the opposite surface of substrate 112 or, as shown in drawing FIG. 12, on the downwardly facing surface of the substrate. Substrate bond pads 76 are placed in electrical communication with ~~chip~~ die bond pads 106 by way of bond

wires 108 preferably extending through aperture 74 as shown and are encapsulated by encapsulant 94. Circuit traces 78 may optionally be located on the downwardly facing surface of substrate 112, by way of substrate tape ~~outline~~ 70 and individual chip circuitry portion 71, for example, and thereby extend outwardly along the downwardly facing surface of substrate 112 whereupon circuit traces 78 may then be routed through the cross-section of substrate 112 or otherwise placed in electrical communication with optional conductive vias or other conductive elements 126 which extend through substrate 112 to the respectively appropriate pad's connective element or solder ball contact pads 114 (i.e., not concave), or optional concave contact pads 114′ located on the opposite or upwardly facing surface of substrate 112. Optionally, electrically connecting substrate bond pads 76 with contact pads 114 or 114′ as discussed earlier, may be achieved by laminating or "sandwiching" circuit traces 78′ within substrate 112 and routing them through substrate 112 in order to electrically connect each laminated circuit trace 78′ to its respective contact pad 114 or optional contact pad 114′. The exemplary upside-down BGA chip package illustrated in drawing FIG. 12 is shown prior to the test pads being disassociated from the chip package along substrate severing line 128. As with circuit traces 78, circuit traces 82 which electrically connect contact pads 114 or optional ~~pads114′~~ contact pads 114′ may be disposed on the upwardly facing surface of substrate 112, or optionally may be laminated within substrate 112 as denoted by trace 82′. Upon reaching its respective test contact pad 84, circuit trace 82, 82′ may then be placed in electrical communication with its respective test contact pad. Specific methods of extending circuit traces through chip package substrates in order to be placed in electrical communication with contact pads or other connective elements are well known within the art.

Please amend paragraph number **[0060]** as follows:

[0060] As shown in drawing FIG. 13, dimension A is the distance between proximate substrates 112 of stacked chip packages ~~which in effect~~ which, in effect, includes the final height of solder ball 116 and two contact pads 114. Dimension A conventionally is approximately .5 mm or greater. Dimension B, the distance between the closest substrate 112 and module

board 120, is conventionally approximately 0.5 mm or greater. Dimension C, which is the total stack height of both or, alternatively, all chip packages above module board 120 if more than two chip packages are stacked together, is conventionally approximately 1.9 mm or greater.

Please amend paragraph number **[0063]** as follows:

[0063] A nonconventionally configured, reduced-profile memory module incorporating exemplary BGA chip packages 110 ~~and110',~~ and 110', as illustrated in drawing FIGS. 10 and 11, is shown in FIG. 14 of the drawings. Reduced-profile BGA chip packages 110A and 110'B, and 110'C and 110D, respectively stacked together and mounted on opposite surfaces 122 and 124 of module board 120, are each configured to have a semiconductor die 92 attached to the same surface of substrate 112 to which solder ball 116 and associated concave solder ball contact pad 114' are attached. BGA chip packages constructed in such a nonconventional "upside-down" manner eliminate the need for encasing the module with a protective cover. This is attributable to the ~~backside~~ back side of each semiconductor die 92 being protected by virtue of being physically positioned between either an adjacent chip package within the same stack or between its respective chip substrate 112 and module board 120. Thus, the added thickness of a protective cover is eliminated, as well as the associated time and costs of applying such a protective cover.

Please amend paragraph number **[0064]** as follows:

[0064] As discussed with respect to reduced-profile or upside-down BGA chip packages 110 and 110' illustrated in drawing FIGS. 10 through 12, such chip packages are preferably constructed, burned-in, and tested in accordance with the earlier-described techniques and procedures incorporating severable test contact pads arranged in conventional patterns such as TSOP pin-out patterns. However, modules such as module 118' as shown in drawing FIG. 14 can be constructed in an "upside-down" manner, with or without concave solder ball contact pads 114', while employing prior conventional construction, burn-in, and testing techniques used in producing BGA chip packages such as representative chip package 10.